Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. - 15. (canceled)

16. (new) A mobile communication terminal comprising:

a microprocessor having registers and an internal memory;

an external memory coupled with the microprocessor;

an antenna receiving a reception data from outside of the mobile communication terminal and transmitting data to outside of the mobile communication terminal; and

an RF circuit converting a frequency of the reception data and the transmission data,

wherein the microprocessor performs a CPU function and a DSP function,

wherein the microprocessor transfers a data from the internal memory to the registers per one cycle when the microprocessor performs the CPU function,

wherein the microprocessor can transfer two data from the memory to the registers per one cycle when the microprocessor performs the DSP function,

wherein the internal memory has a first internal memory and a second internal memory,

wherein the microprocessor can transfer two data from the first and second internal memories in parallel when the microprocessor performs the DSP function, and

wherein the external memory is shared by the CPU function and DSP function.

17. (new) A mobile communication terminal according to claim 16, wherein the external memory is memory outputting data based on a clock.

18. (new) A mobile communication terminal according to claim 16,

wherein the microprocessor outputs a first data signal corresponding to the transmission data, a first frame sync signal and a first basic clock in parallel in order to transmit the transmission data from the antenna, and

wherein the microprocessor receives a second data signal corresponding to the reception data, a second frame sync signal and a second basic clock in parallel in order to perform the reception data.

19. (new) A mobile communication terminal according to claim 18,

wherein the first and second data signals are transferred via different signal lines,

wherein the first and second sync signals are transferred via different signal lines, and

wherein the first and second basic clock are transferred via different signal lines.

20. (new) A mobile communication terminal according to claim 16

wherein the microprocessor performs a shift operation by using the CPU function and

wherein the microprocessor performs a FIR filter operation by using the DSP function.

21. (new) A mobile communication terminal according to claim 16

wherein the reception data received by the antenna is performed in the microprocessor, and

wherein when the microprocessor performs the reception data by using the DSP function, a part or all the data performed by using the DSP function is stored in the external memory.

22. (new) A mobile communication terminal according to claim 16, wherein the external memory stores the program for using both the DSP function and the CPU function.

23. (new) A mobile communication terminal according to claim 16,

wherein the microprocessor further has an arithmetic logic unit, and

wherein the arithmetic logic unit performs an address operation for both of the CPU function and the DSP function.

24. (new) A mobile communication terminal comprising:

a microprocessor having registers and an internal memory;

an external memory coupled to the microprocessor;

an antenna receiving a reception data from outside of the mobile communication terminal and transmitting a transmission data to outside of the mobile communication terminal, and

an RF circuit converting a frequency of the reception data and the transmission data,

wherein the microprocessor performs a program by using a CPU function or a DSP function,

wherein the internal memory has a first internal memory and a second internal memory,

wherein the microprocessor can transfer two data from the first and second internal memories in parallel when the microprocessor performs the DSP function, and

wherein the microprocessor performs the reception data by using the DSP function, the external memory stores a part or all of the data performed by using the DSP function.

25. (new) A mobile communication terminal according to claim 24, wherein the external memory is memory outputting data based on a clock.

26. (new) A mobile communication terminal according to claim 25,

wherein the microprocessor outputs a first data signal corresponding to the transmission data, a first frame sync signal and a first basic clock in parallel in order to transmit the transmission data from the antenna, and

wherein the microprocessor receives a second data signal corresponding to the reception data, a second frame sync signal and a second basic clock in parallel in order to perform the reception data.

27. (new) A mobile communication terminal according to claim 26,

wherein the first and second data signals are transferred via different signal lines,

wherein the first and second sync signals are transferred via different signal lines, and

wherein the first and second basic clocks are transferred via different signal lines.

28. (new) A mobile communication terminal according to claim 24,

wherein the microprocessor performs a shift operation using the CPU function, and

wherein the microprocessor performs a FIR filter operation by using the DSP function.

29. (new) A mobile communication terminal according to claim 24, wherein the external memory is shared by the CPU function and the DSP function.

30. (new) A mobile communication terminal according to claim 24, wherein the external memory stores the program for using both the DSP function and the CPU function.

31. (new) A mobile communication terminal according to claim 24, wherein the microprocessor further has an arithmetic logic unit, and

wherein address operations for both of the CPU function and the DSP function are performed by the common arithmetic logic unit.

32. (new) A mobile communication terminal according to claim 24,

wherein the microprocessor transfers a data from the internal memory to the registers per one cycle when the microprocessor performs the CPU function, and

wherein the microprocessor can transfer two data from the memory to the registers per one cycle when the microprocessor performs the DSP function.